CLAIMS

1. An electronic device, comprising:

a memory structure comprising an integer *M* of memory word slots, wherein each memory word slot is operable to store an integer *N* of bits;

a scan storage circuit, operable to receive a scan word having a number of bits less than *MxN*; and

control circuitry for causing successive scan words to be written into the scan storage circuit, for causing successive scan words to be written from the scan storage circuit into the memory structure, and for causing successive scan words to be read from the memory structure into the scan storage circuit.

2. The electronic device of claim 1 wherein the scan storage circuit is operable to receive a scan word consisting of *N* bits.

3. The electronic device of claim 2 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit.

4. The electronic device of claim 3 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit.

5. The electronic device of claim 4 wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in parallel.

6. The electronic device of claim 5:

wherein the successive scan words to be written into the scan storage circuit comprise a test sequence; and

further comprising circuitry for comparing the successive scan words to be read from the memory structure to the test sequence.

7. The electronic device of claim 6:

wherein each memory word slot is operable to store the integer *N* of bits in a corresponding set of *N* memory cells; and

wherein each set of *N* memory cells comprises *N* latches.

8. The electronic device of claim 7 wherein each of the *N* latches comprises:

a first inverter having an input providing an input to the latch and an output providing an output of the latch; and

a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch.

9. The electronic device of claim 7 wherein each memory word slot is operable to store the integer *N* of bits in a corresponding set of *N* memory cells; and

wherein each set of *N* memory cells is operable to store incoming data without responding to a clock transition.

10. The electronic device of claim 9 wherein *N* is selected from a group consisting of 128, 64, 32, 16, 8, and 4.

11. The electronic device of claim 1 wherein the control circuitry is further for causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit.

12. The electronic device of claim 1 wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit.

13. The electronic device of claim 1 wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in parallel.

14. The electronic device of claim 1:

wherein the scan storage circuit comprises a serial shift storage circuit for serially causing each successive scan word to be read from the scan storage circuit during a same time period as a corresponding successive scan word is written into the scan storage circuit; and

wherein the scan storage circuit further comprises circuitry for causing each successive scan word to be written from the scan storage circuit into the memory structure in parallel, and for causing each successive scan word to be read from the memory structure into the scan storage circuit in parallel.

15. The electronic device of claim 1:

wherein each memory word slot is operable to store the integer N of bits in a corresponding set of N memory cells; and

wherein each set of N memory cells comprises N latches.

16. The electronic device of claim 15 wherein each of the N latches comprises:

a first inverter having an input providing an input to the latch and an output providing an output of the latch; and

a second inverter having an input connected to the output of the first latch and having an output connected to the input of the first latch.

17. The electronic device of claim 1 wherein the memory structure, the scan storage circuit, and the control circuitry are all in a single integrated circuit.

18. A method of operating an electronic device, the device comprising a memory structure comprising an integer *M* of memory word slots, wherein each memory word slot is operable to store an integer *N* of bits;

causing successive scan words to be written into a scan storage circuit, the scan storage circuit operable to receive a scan word having a number of bits less than *MxN*;

causing successive scan words to be written from the scan storage circuit into the memory structure; and

causing successive scan words to be read from the memory structure into the scan storage circuit.

19. The method of claim 18 wherein the scan storage circuit is operable to receive a scan word consisting of *N* bits.

20. The method of claim 19 and further comprising causing each successive scan word to be read from the scan storage circuit during a same time period as causing corresponding successive scan words to be written into the scan storage circuit.

21. The method of claim 19 and further comprising causing each successive scan word to be serially read by shifting bits out from the scan storage circuit during a same time period as causing corresponding successive scan words to be serially written by shifting bits into the scan storage circuit.

22. The method of claim 21:

wherein the step of causing successive scan words to be written from the scan storage circuit into the memory structure comprises writing each successive scan word from the scan storage circuit into the memory structure in parallel; and

wherein the step of causing successive scan words to be read from the memory structure into the scan storage circuit comprises writing each successive scan word from the memory structure into the scan storage circuit in parallel.

*****